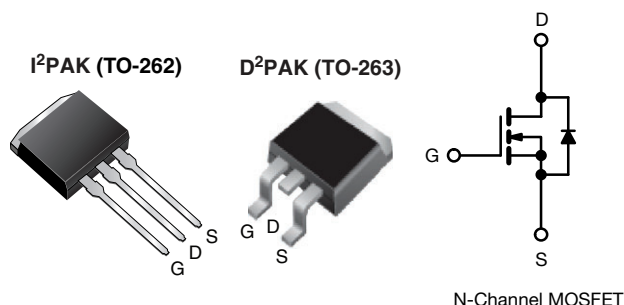


Power MOSFET



FEATURES

- Advanced process technology
- Surface-mount (IRFZ48S, SiHFZ48S)
- Low-profile through-hole (SiHFZ48L)
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface-mount application.

The through-hole version (SiHFZ48L) is available for low-profile applications.

PRODUCT SUMMARY

V _{DS} (V)	60	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.018
Q _g max. (nC)	110	
Q _{gs} (nC)	29	
Q _{gd} (nC)	36	
Configuration	Single	

ORDERING INFORMATION

Package	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHFZ48S-GE3	SiHFZ48L-GE3
Lead (Pb)-free	IRFZ48SPbF	-
	IRFZ48STRLPbF	-

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current ^f	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^{a, e}	I _{DM}	290	
Linear derating factor		1.3	W/°C
Single pulse avalanche energy ^{b, e}	E _{AS}	100	mJ
Maximum power dissipation	P _D	T _C = 25 °C	W
		T _A = 25 °C	
Peak diode recovery dv/dt ^{c, e}	dv/dt	4.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

b. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

c. V_{DD} = 25 V, Starting T_J = 25 °C, L = 22 μH, R_g = 25 Ω, I_{AS} = 72 A (see fig. 12)

d. I_{SD} ≤ 72 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C

e. 1.6 mm from case

f. Uses IRFZ48, SiHFZ48 data and test conditions

g. Calculated continuous current based on maximum allowable junction temperature

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	°C / W
Maximum junction-to-case (drain)	R_{thJC}	-	0.8	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$ ^c	-	0.060	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ °C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 43\text{ A}$ ^b	-	-	0.018	Ω
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 43\text{ A}$ ^b	27	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 ^c	-	2400	-	pF
Output capacitance	C_{oss}		-	1300	-	
Reverse transfer capacitance	C_{rss}		-	190	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 72\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	110	nC
Gate-source charge	Q_{gs}		-	-	29	
Gate-drain charge	Q_{gd}		-	-	36	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 72\text{ A}$, $R_g = 9.1\text{ }\Omega$, $R_D = 0.34\text{ }\Omega$, see fig. 10 ^{b, c}	-	8.1	-	ns
Rise time	t_r		-	250	-	
Turn-off delay time	$t_{d(off)}$		-	210	-	
Fall time	t_f		-	250	-	
Internal source inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	50 ^c	A
Pulsed diode forward current ^a	I_{SM}		-	-	290	
Body diode voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 72\text{ A}$, $V_{GS} = 0\text{ V}$ ^b	-	-	2.0	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = 72\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ ^{b, c}	-	120	180	ns
Body diode reverse recovery charge	Q_{rr}		-	0.5	0.8	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. Uses IRFZ48, SiHFZ48 data and test conditions
d. Calculated continuous current based on maximum allowable junction temperature



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

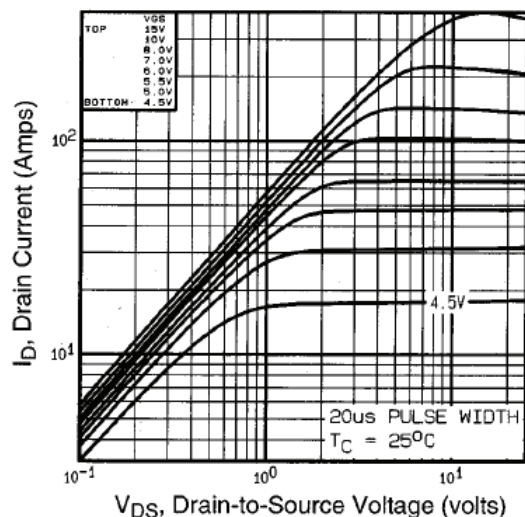


Fig. 1 - Typical Output Characteristics
B

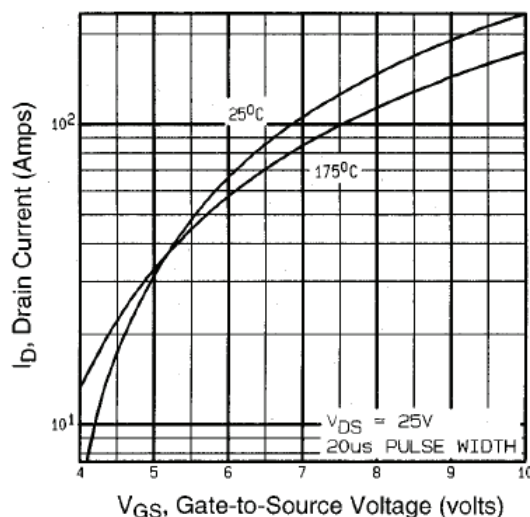


Fig. 3 - Typical Transfer Characteristics

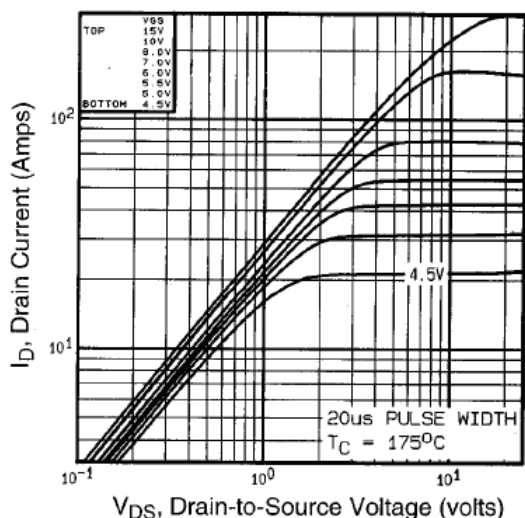


Fig. 2 - Typical Output Characteristics

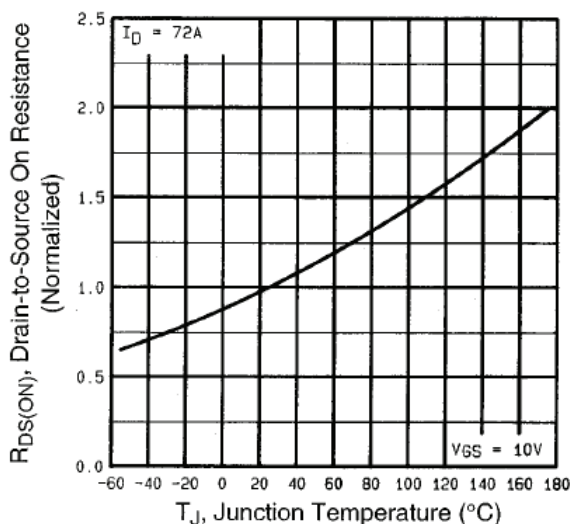
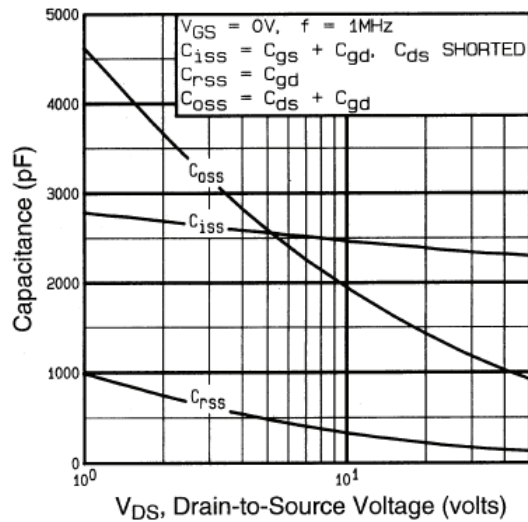
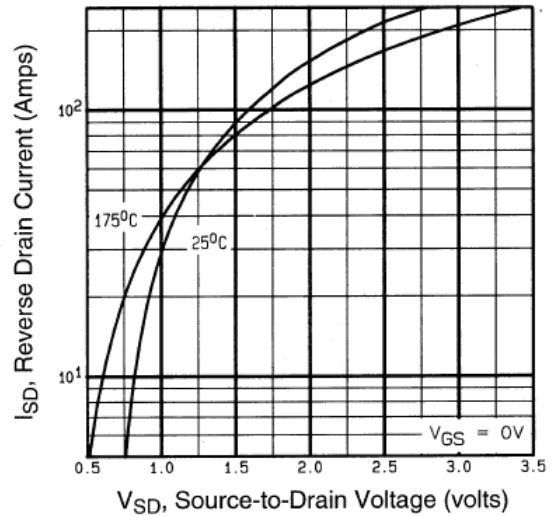
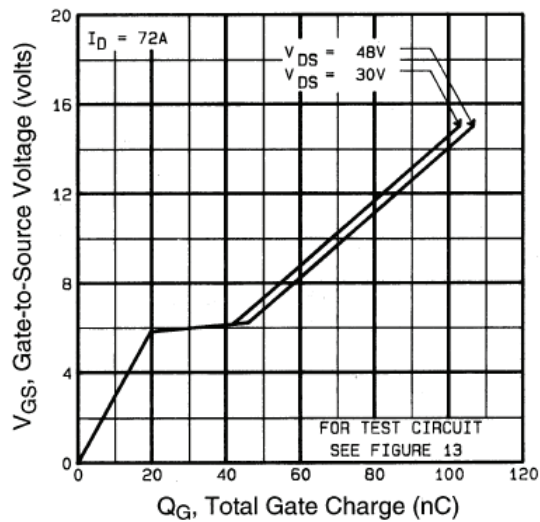
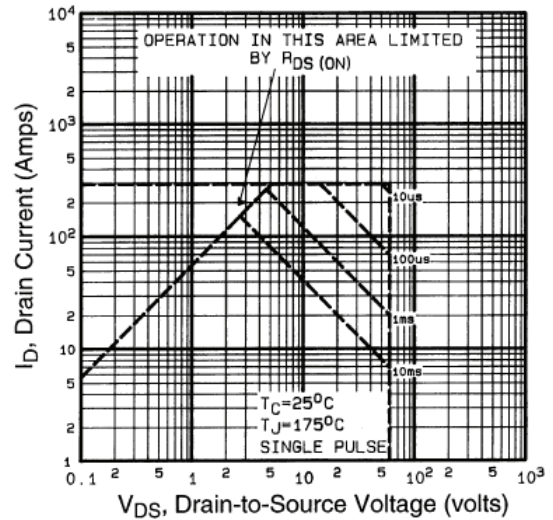


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

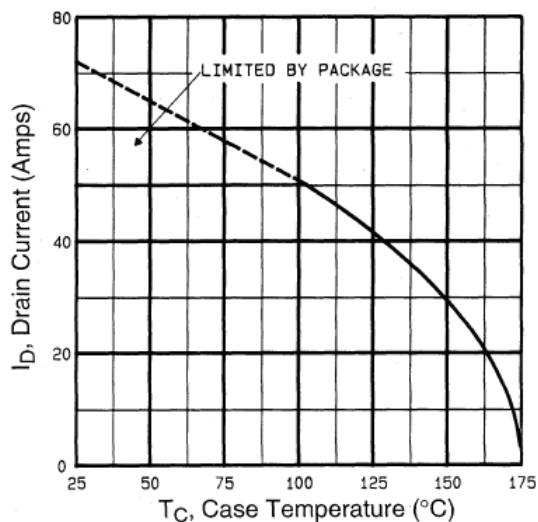


Fig. 9 - Maximum Drain Current vs. Case Temperature

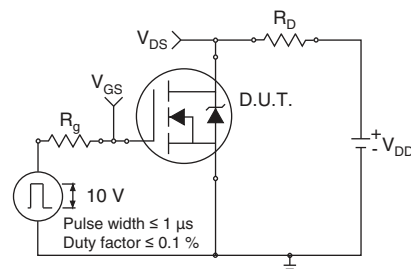


Fig. 10a - Switching Time Test Circuit

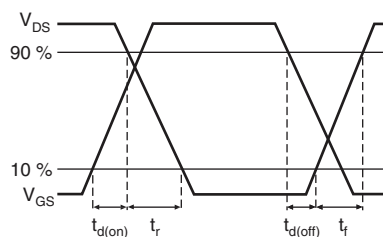


Fig. 10b - Switching Time Waveform

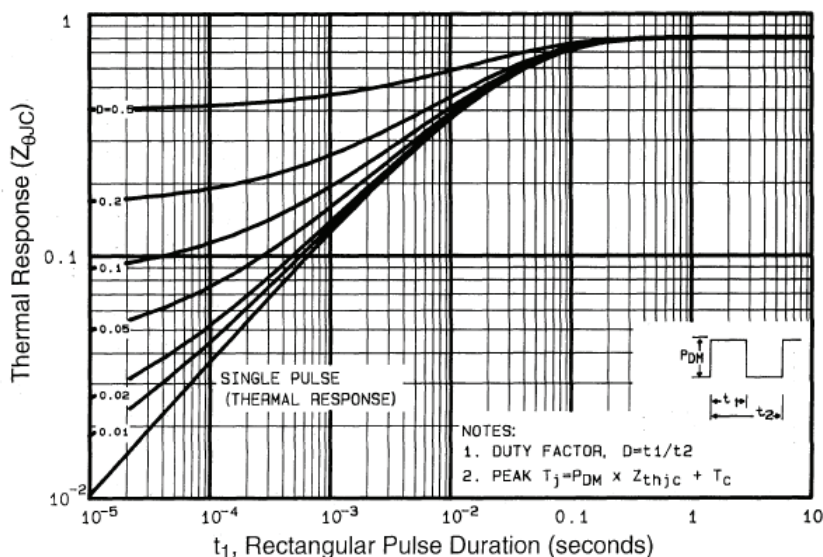


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

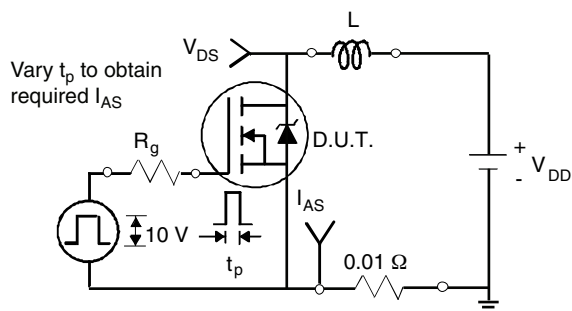


Fig. 12a - Unclamped Inductive Test Circuit

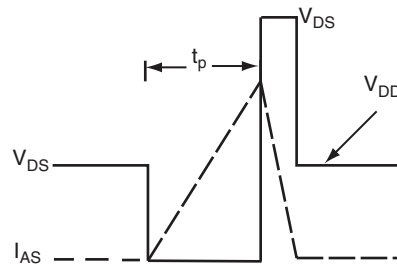
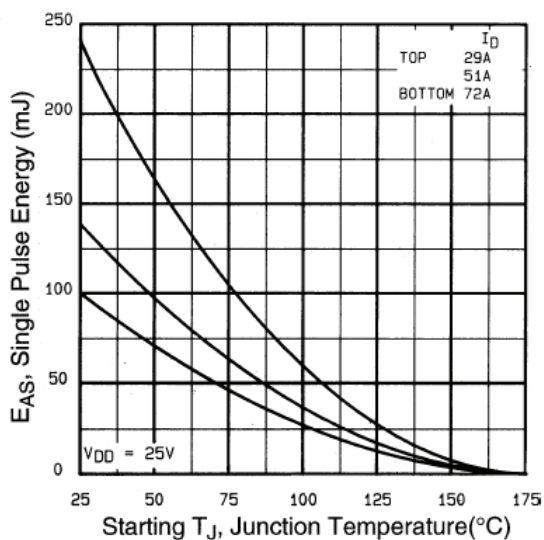
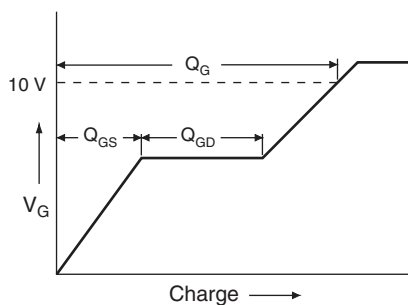
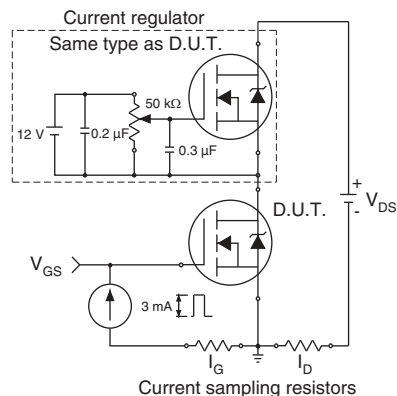
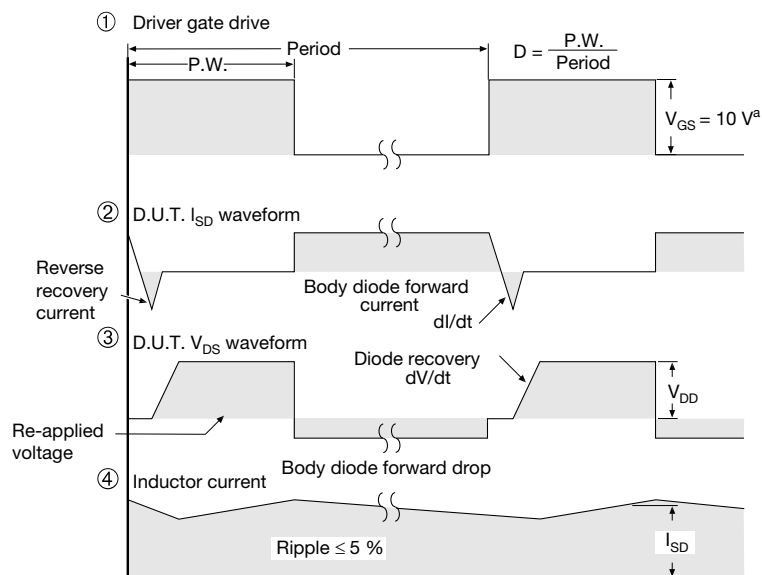
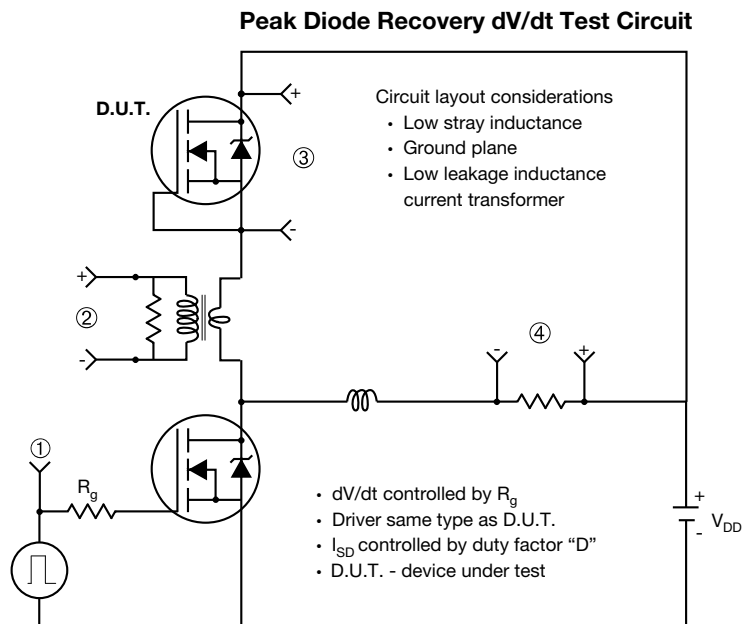


Fig. 12b - Unclamped Inductive Waveforms

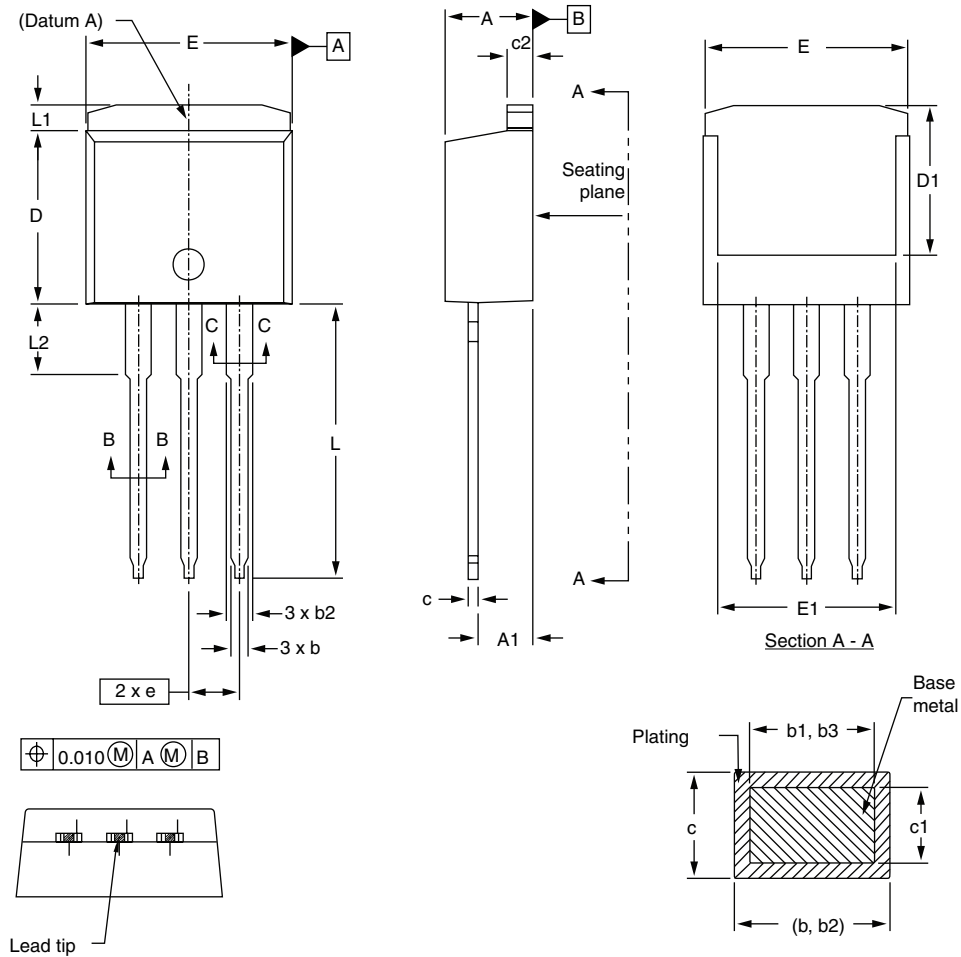

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Maximum Avalanche Energy vs. Drain Current

Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

I²PAK (TO-262) (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

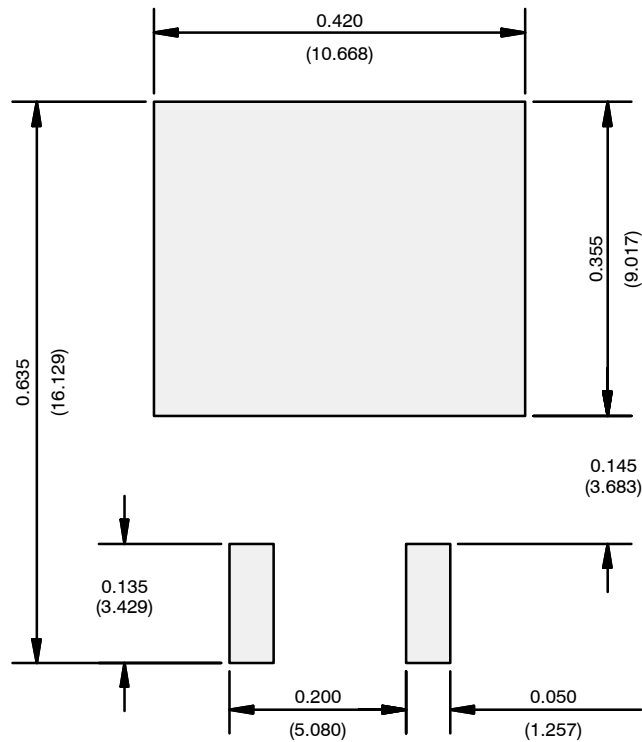
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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